Official Amendment
Serial No. 09/943,078
Docket No. MIO 0083 PA/40509.12

Amendments to the Claims:

This listing of claims will replace all prior versions, and lists, of claims in the application:

Claims 1-49. (Canceled)

50. (New) A method of fabricating a semiconductor device comprising:
forming a damascene trench in a first dielectric layer over a base substrate, said damascene trench having a gate area and a local interconnect area;
depositing a conductive layer over said base substrate such that said damascene trench is filled with a conductive material;
planarizing said device to define a damascene structure including a damascene gate structure and a damascene local interconnect structure electrically coupled by said conductive material within said damascene trench, wherein said damascene local interconnect structure forms a direct connection to said base substrate;
providing at least one implant contact within a plug area, wherein said plug area is located at least partially beneath and in contact with said damascene local interconnect structure; and
forming doped source/drain regions in said base substrate adjacent and lateral to said damascene gate structure and said damascene local interconnect structure.

51. (New) The method of fabricating a semiconductor device of claim 50, further comprising:
forming an isolation trench in said base substrate before said first dielectric layer is formed.

52. (New) The method of fabricating a semiconductor device of claim 51, wherein at least a portion of said damascene trench partially overlies said isolation trench.

Official Amendment
Serial No. 09/943,078
Docket No. MIO 0083 PA/40509.12

53. (New) The method of fabricating a semiconductor device of claim 51, further comprising:
forming a plurality of gate areas in said damascene trench.

54. (New) The method of fabricating a semiconductor device of claim 51, further comprising:
forming a plurality of local interconnect areas in said damascene trench.

55. (New) A method of fabricating a semiconductor device comprising:
forming a damascene trench in a first dielectric layer over a base substrate, said damascene trench having a gate area and a local interconnect area;
depositing a conductive layer over said base substrate such that said damascene trench is filled with a conductive material, wherein said conductive material comprises a polysilicon material;
planarizing said device to define a damascene structure including a damascene gate structure and a damascene local interconnect structure electrically coupled by said conductive material within said damascene trench, wherein said damascene local interconnect structure forms a direct connection to said base substrate;
forming a silicide layer over said polysilicon material within said gate area of said damascene trench; and
forming doped source/drain regions in said base substrate adjacent and lateral to said damascene gate structure and said damascene local interconnect structure.

56. (New) A method of fabricating a semiconductor device comprising:
forming a damascene trench in a first dielectric layer over a base substrate, said damascene trench having a gate area and a local interconnect area;
depositing a conductive layer over said base substrate such that said damascene trench is filled with a conductive material;

planarizing said device to define a damascene structure including a damascene gate structure and a damascene local interconnect structure electrically coupled by said conductive material within said damascene trench, wherein said damascene local interconnect structure forms a direct connection to said base substrate;

forming lightly doped drain regions in said base substrate after removing said first dielectric layer, said lightly doped drain regions formed within said base substrate adjacent and lateral to said damascene gate structure and said damascene local interconnect structure; and

forming doped source/drain regions in said base substrate adjacent and lateral to said damascene gate structure and said damascene local interconnect structure.

57. (New) The method of claim 56 further comprising:

forming spacers against the vertical walls of said damascene gate structure and said damascene local interconnect structure.

58. (New) A method of fabricating a semiconductor device comprising:

forming an isolation trench in a base substrate;

forming a first dielectric layer over said base substrate;

forming a first patterned mask over said first dielectric layer;

etching through said first dielectric layer to said base substrate in areas defined by said first patterned mask to define a damascene trench in said first dielectric layer, said damascene trench having a gate area and a local interconnect area and positioned such that at least a portion of said damascene trench at least partially overlies said isolation trench;

stripping said first patterned mask from said first dielectric layer;

growing an oxide layer on said base substrate, said oxide layer within said gate area of said damascene trench defining a gate oxide layer;

forming a second patterned mask over said semiconductor device, said second patterned mask arranged to expose at least a portion of said oxide layer within said local interconnect area, wherein said damascene local interconnect structure forms a direct connection to said base substrate;

etching away the exposed portion of said oxide layer within said damascene trench;

providing at least one contact implant within a plug area in said base substrate, wherein said plug area is located at least partially beneath and in contact said damascene local interconnect structure;

stripping said second patterned mask from said semiconductor device;

depositing a conductive layer comprising a conductive material over said device such that said conductive layer fills said damascene trench;

planarizing said conductive layer down to the surface of said dielectric layer;

removing said first dielectric layer to define a damascene gate structure and a damascene local interconnect structure;

forming lightly doped drain regions in said base substrate adjacent and lateral to said damascene gate structure and said damascene local interconnect structure;

depositing a spacer layer over said device;

anisotropically etching said spacer layer such that spacers are formed over the portions of said base substrate where said lightly doped drain regions are formed; and

forming doped source/drain regions in said base substrate after forming said spacers such that said base substrate is doped more deeply into said base substrate adjacent and lateral to said spacers than into said base substrate underneath said spacers.